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ADAPTATION OF APPLE-II ADC BOARDS FOR IBM-PC MICROCOMPUTERS

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This project allows analog-to-digital conversor boards (ADC) originally developed for Apple-II microcomputers to be used in IBM-PC compatible microcomputers. The low cost design uses an Apple-II standard slot and a simple auxiliary circuit assembled in a standard IBM-PC board. An external trigger circuit is provided for monitoring assyncronous events.

Typeset Using *REVTEX*

ADC [1, 2] boards have I/O ports accessed by the microcomputer for controlling and for reading data from the boards. In order to use an ADC board developed for the Apple-II in a IBM-PC microcomputer, we must emulate in the IBM-PC the necessary Apple-II bus signals through an auxiliary circuit. The hardware connections were made assembling an Apple slot and an auxiliary circuit in a standard IBM-PC board, as shown in Fig. 1.

In a IBM-PC, the main microprocessor is typically an Intel- 8088 or others from the 8086 family. These microprocessors have separated instructions for accessing either the memory or I/O devices [3]. Therefore, there are four signals indicating the type of operation to be performed [4]: $\overline{MEMR}$ (memory read), $\overline{MEMW}$ (memory write), $\overline{IOR}$ (I/O read), and $\overline{IOW}$ (I/O write). Thus, we have separated set of addresses for memory locations and for I/O devices, Fig. 2(a).

The Apple-II 6502 [5] microprocessor has no distinct instructions for accessing memory and I/O devices. Thus a single set of addresses is shared by memory and I/O devices, Fig. 2(b).

A $\overline{DEVICE\ SELECT}$ signal is activated in the n^{th} slot when an I/O read/write operation is performed by the Apple in an address between \$C080 + \$n0 and \$C08F + \$n0 [6].

There are also differences in the bus timing processes. In the IBM-PC the $\overline{IOW}$ (or $\overline{IOR}$) signal is enabled just after the other signals used in the operation are set ready and is the first one to be disabled, indicating that the I/O operation is finished [4]. In the Apple-II, the $R/\overline{W}$ must be set before the $\overline{DEVICE\ SELECT}$ and disabled after it [5].

The auxiliary circuit is shown in Fig. 3, arranged in four parts, for easier reference:

A) Clock circuit: This TTL-RC oscillator generates an 1 MHz signal, emulating the ϕ_0 Apple-II clock signal. This signal is necessary for those ADC [2] that uses the

Apple-II clock signal as a timing conversion base. So, ADC boards can be used in different IBM-PCs, independent of their clock frequencies.

B) Device Select Emulator (DSE): This section of the circuit generates the Apple-II $\overline{DEVICE\ SELECT}$ signal, activated through an $\overline{IOW}$ ($\overline{IOR}$) operation in the addresses from \$300 to \$30F (J1...J6, in the position 1). The inverters (IC8) are needed only when the above addresses are not available for any reason. An example to change the addresses from \$300 - \$30F to \$320 - \$32F follows:

When the IBM-PC microprocessor is addressing in the range from \$320 to \$32F, we have the following states in the bus:

A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

1 1 0 0 1 0 - - - -

But since the DSE recognizes only the states

A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

1 1 0 0 0 0 - - - -

the bit A5 must be inverted with J2 in the position 2.

We have inserted two standard TTL NAND inverters in the $\overline{DEVICE\ SELECT}$ output as a delay time, constraining this line to be activated only after the $R/\overline{W}$ line is set up.

C) $R/\overline{W}$ Emulator (RWE): The monostable circuit IC7 emulates the Apple-II $R/\overline{W}$ signal using the IBM-PC $\overline{IOW}$ signal. The RWE was designed to generate a pulse width larger than the $\overline{DEVICE\ SELECT}$ signal width for any IBM-PC clock frequency.

D) External Trigger: This circuit is enabled by the jumper J7 in the position 1. The logic state of the four external triggers is determined by the most significant

bits of the contents of any port from \$308 to \$30F. This circuit may be expanded using also the less significant bits, inserting another IC similar to IC6. The addresses used are shown in Table I.

As no structural modifications were done neither in the ADC board nor in the IBM-PC, the design shown to be inexpensive and easy to assemble. An improvement is the external trigger circuit, that allows monitoration of signals due to assyncronous events.

ACKNOWLEDGMENTS

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REFERENCES

[1] *ADC Manual*, Applied Engineering, Carrollton, Texas, 1984.

[2] *AM13 ADC Manual*, Anamed Ltda, São Paulo, Brazil, 1985.

[3] S. Holzner. *Advanced Assembly Language for the IBM-PC.* Brady Books, Simon & Schuster, Inc., 1990.

[4] C. L. Morgan & M. W. Morgan. *8086/8088 16-bit Microprocessors Primer*, McGraw-Hill Co., 1982.

[5] *Apple-IIe Reference Manual*, Apple Computer Inc., 1982.

[6] J. W. Coffron. *The Apple Connection*, Sybex Inc., 1982.

[7] P. Horowitz, W. Hill. *The Art of Electronics*, Cambridge University Press, Cambridge, 1983.

FIGURES

FIG. 1. The Apple slot assembled in a IBM-PC standard board.

FIG. 2. a) IBM-PC memory and I/O maps b) Apple memory map

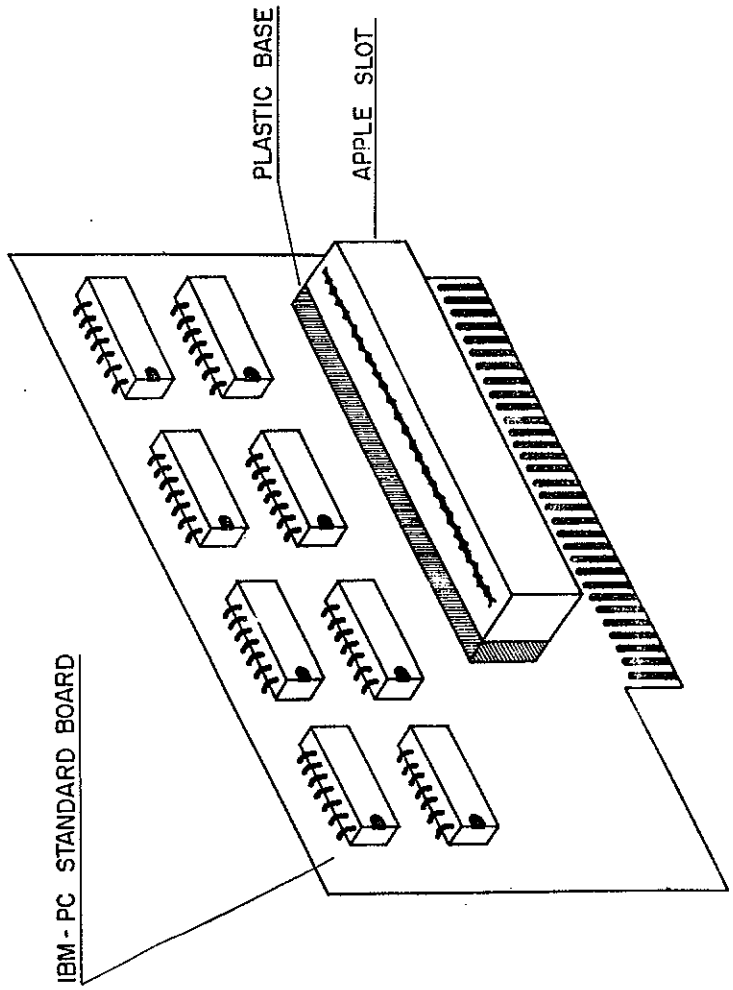
FIG. 3. Auxiliary interfacing circuit. A) Clock circuit B)Device Select emulator C) $R/\overline{W}$ emulator D)External trigger.

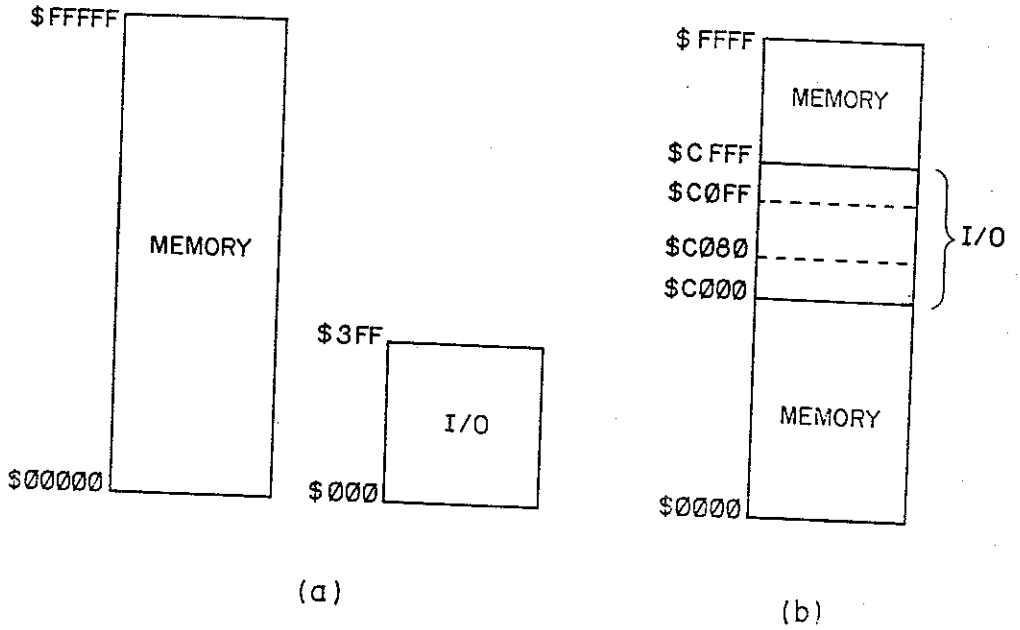
TABLES

TABLE I. The equivalence of addresses established between the Apple-II slots and the IBM-PC.

Apple-II addresses, $n = 0,...7$	IBM-PC addresses without trigger	IBM-PC addresses with trigger
\$C080 + \$n0	\$300	\$300
\$C081 + \$n0	\$301	\$301
...	...	...
\$C087 + \$n0	\$307	\$307
\$C088 + \$n0	\$308	N/A
\$C089 + \$n0	\$309	N/A
...	...	...
\$C08F + \$n0	\$30F	N/A

Fig. 1




$FFFFF
MEMORY
$00000
$3FF
I/O
$000
(a)
$FFFF
MEMORY
$CFFF
$C0FF
$C080
$C000
I/O
MEMORY
$0000
(b)

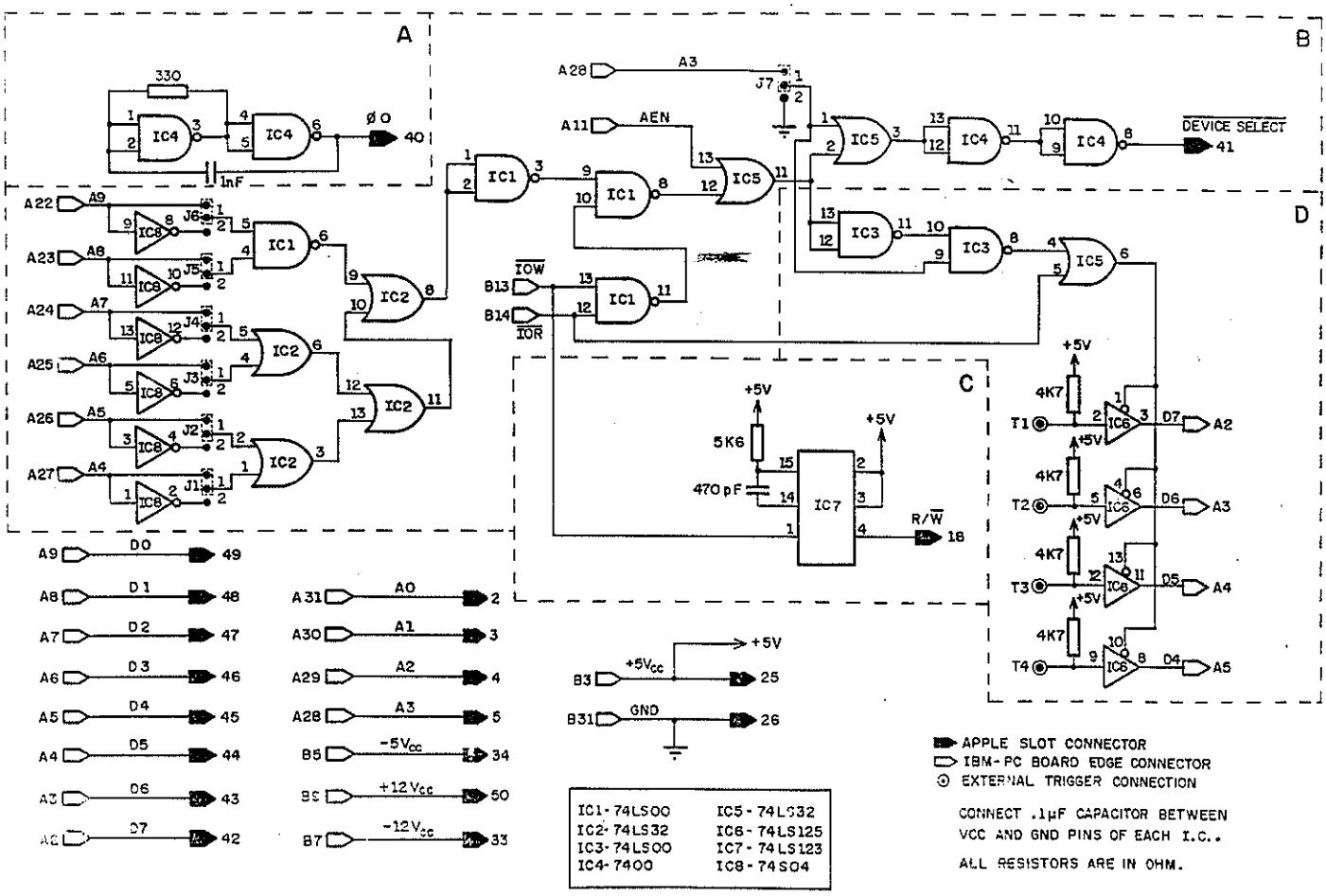

A
B
C
D
330
IC4
ø0
40
1nF
A22
A23
A24
A25
A26
A27
IC8
IC1
IC2
A28
A3
J7
A11
AEN
IC5
IC3
DEVICE SELECT
41
B13
B14
IOW
IOR
+5V
5K6
470pF
IC7
R/W
18
4K7
T1
T2
T3
T4
IC6
D7
D6
D5
D4
A2
A3
A4
A5
A9
D0
49
A8
D1
48
A7
D2
47
A6
D3
46
A5
D4
45
A4
D5
44
A3
D6
43
A2
D7
42
A31
A0
2
A30
A1
3
A29
A2
4
A28
A3
5
B5
-5Vcc
34
B3
+12Vcc
50
B7
-12Vcc
33
B3
+5Vcc
25
B31
GND
26
APPLE SLOT CONNECTOR
IBM-PC BOARD EDGE CONNECTOR
EXTERNAL TRIGGER CONNECTION
CONNECT .1µF CAPACITOR BETWEEN VCC AND GND PINS OF EACH I.C..
ALL RESISTORS ARE IN OHM.
IC1-74LS00
IC2-74LS32
IC3-74LS00
IC4-7400
IC5-74LS32
IC6-74LS125
IC7-74LS123
IC8-74S04

Fig 3